Universal Test-Solution for IC Verification and Characterization

Features:

- 8 Power supplies (±16.5 V, 100 mA)
- 4 Reference sources (±12 V)
- 2 Current sources (±100 mA)
- 2 High performance analog signal paths
- 3 Measurement paths (up to 24 bit)
- Fully programmable digital interface
- Customizable software

Application

- Lab verification and characterization including:
  - Dataconverters (ADC, DAC)
  - Amplifiers (OPA, INA)
  - Mixed-Signal ASICs
  - and many more

Overview

The eyTST-01 is a universal test solution for the verification and characterization of electrical systems. Its particularly small form factor makes it ideal for IC verification as it fits underneath a probe station or inside a temperature chamber. Minimal wiring is required to set up the eyTST-01.
All resources including digital have shortest possible wiring to the device-under-test to minimize parasitic effects, such as digital signal delays or analog signal distortion.
Software is surely supporting all functions that are listed as features. Additional customization can optionally be done through plug-ins. The software also provides calibration routines, which allow optimal performance. Device specific software and firmware is available on www.eesy-ic.com.

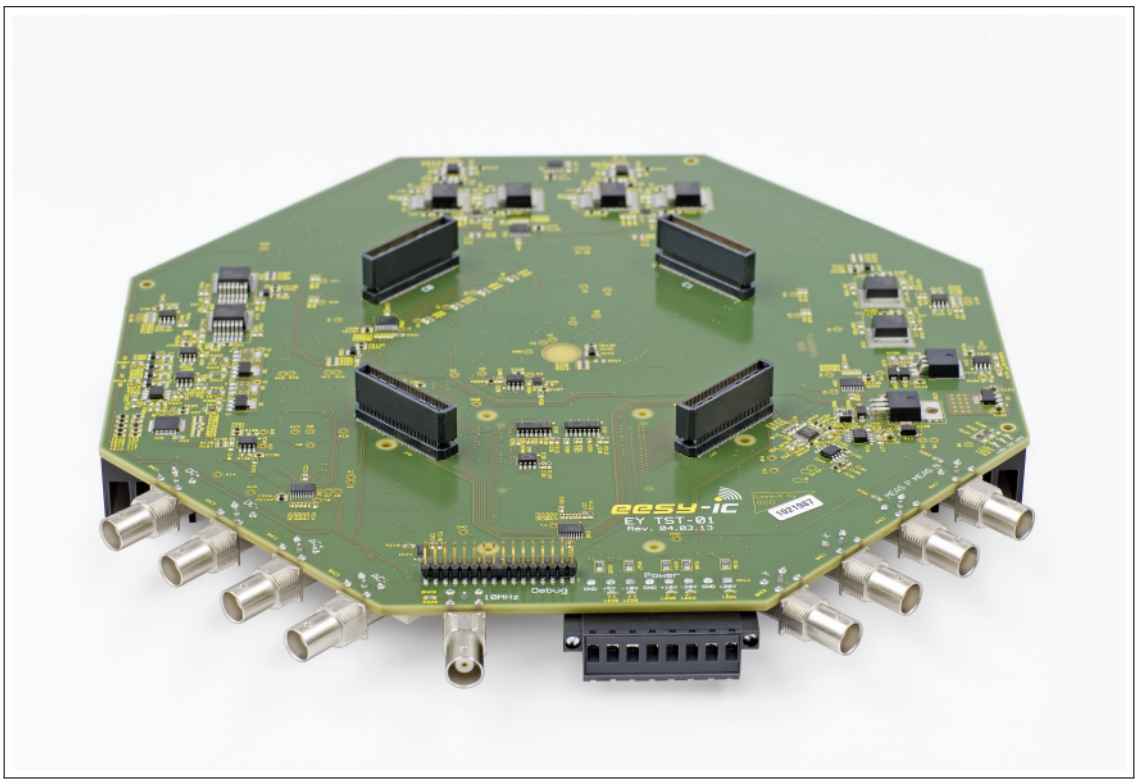

Figure 1: Photograph of eyTST-01(revA)

Contents

1 Description

eyTST-01 is a test solution that provides a series of programmable resources, consisting of 8 power supplies, 4 reference voltages, 2 current sources, 2 analog signal paths, 3 measurement paths and digital resources. The resources are routed to the connectors C0, C1, C2 and C3, which can be used to directly connect a printed circuit board for an electrical device under test (DUT). Alternatively, optional cables can be used to connect to other devices. C0 and C1 are used for the connection of the supplies and analog resources. Please be aware that connector C0 is rotated by 180 degrees in order to avoid mixing up signals and supplies while mounting the printed circuit board. More details on the contactors can be found in the section on DUT connectors.

A FPGA board is connected to the eyTST-01 which provides a USB connection to the computer. The provided software uses the USB interface to control the available resources. It further provides a clock generator, memory and digital resources, which are made available for the device under test through the contactors C2 and C3. A BNC connector, which is marked with 10 MHz, is available and can be used to provide an optional 10 MHz reference clock or trigger signals for external equipment. In addition, a contactor labeled debug is connected to the FPGA. Any digital signal from the FPGA can be routed to the debug connector to simplify the FPGA development. For more details see the section on digital resources.

The eyTST-01 is supplied through the power connector. The analog circuitry and the DUT supplies require ±20 V input supplies. Optionally, additional input supplies can be connected to the ports ±USER. These additional input supplies can be used to source the DUT supplies P3, P4, P5 and P6 when high current and low voltage DUT supplies are required. This limits the heat generation on the eyTST-01 and increases the resource stability. The digital circuitry operates from a 5V supply. A triple power supply such as the E3631A from Agilent can be used. The digital resources however have a 3.3 V high level. Additional board supplies are generated, which are 3.3 V, 15 V and -15 V. Their functionality is visualized with LED lights.

DUT supply currents, DUT supply voltages, DUT references and their currents can be verified with the measurement path. Eight measurement channels and three measurement paths are available for the DUT. The High Speed Measurement Unit operates at 1 MSPS with a resolution of 18 bit and the High Resolution path provides a 24 bit resolution at 10 Hz. Alternatively, an external multimeter can be connected to the BNC connectors MEAS_P and MEAS_N, which might be useful for board calibration.

Finally, two output BNC connectors X and Y are provided. A voltage ramp is generated on eyTST-01 which, for example, can be used to verify the transfer function of Analog-to-Digital converters (ADC). Meanwhile a 5 bit DAC is connected to Y, which is controlled by the FPGA. Y can, for example, express the LSBs of the ADC. Connecting X and Y to a oscilloscope can make the ADC transfer function visible.

For the normal operation, only the input power cables and the USB cable are required. All cables exit to one side of the board for a simplified operation of the board underneath a manual probe station or inside a temperature chamber.

If eyTST-01 is used together with a DUT PCB, then the builtup of PCBs would look as illustrated in Figure 2. The DUT PCB might be sized, so that a thermostream can fit easily on top of it. A recommended layout can be found on www.eesy-ic.com.

2 Absolute Maximum Ratings

The maximum ratings are listed in Table 2.

MEAS_P, MEAS_N, X, Y, MEAS_I and 10 MHz are output ports. Do not apply voltage or current sources to these pins.

Protection features are applied on the eyTST-01. Nevertheless, it includes electrically sensitive devices and can be destroyed with Electro Static Discharge (ESD) or with electrical overstress. The board supplies (±20 V, +5 V and optionally ±USER) need to be applied before programming any DUT resources.

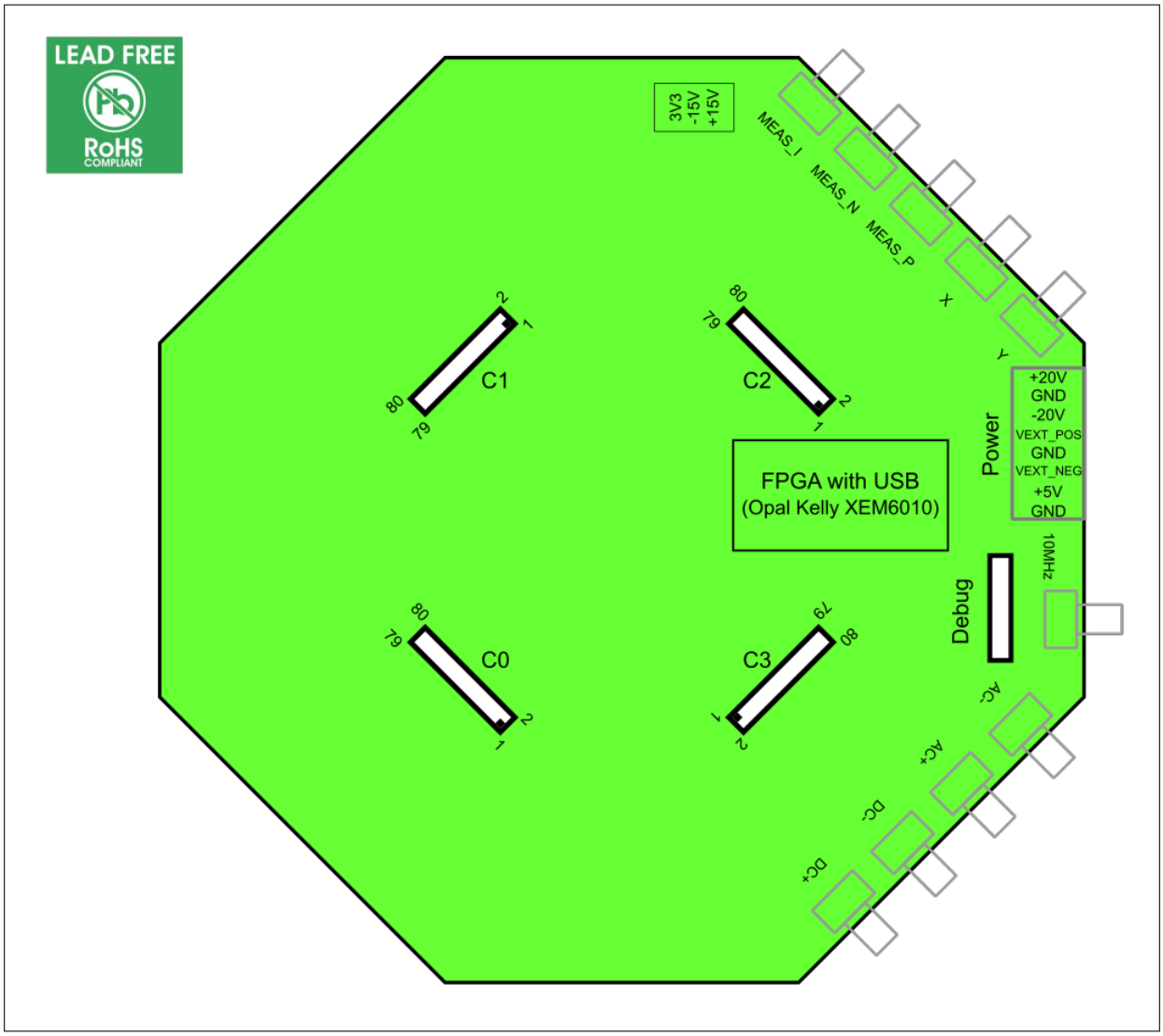

Figure 2: eyTST-01 and its connectors

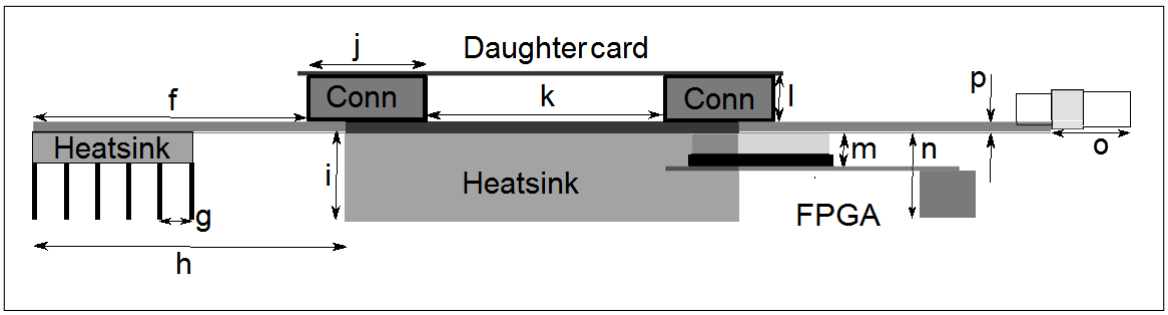

Figure 3: Side view of a test solution with eyTST-01

Parameter	Value	Unit	Parameter	Value	Unit
f	70	mm	l	15	mm
g	8.1	mm	m	7.2	mm
h	80	mm	n	19.8	mm
i	22	mm	o	22	mm
j	30	mm	p	3.1	mm
k	60	mm			

Table 1: Dimensions of Side View

Parameter	Comment	Min	Typ	Max	Unit
+20V	to GND	-0.3		21	V
-20V	to GND	-21		0.3	V
+USER	to GND	-0.3		24	V
-USER	to GND	-24		0.3	V
+5V	to GND	-0.3		5.5	V
DC Analog Inputs	DC+, DC- to AGND	-12.5		12.5	V
AC Analog Inputs	AC+, AC- to AGND	-12.5		12.5	V

Table 2: Absolute maximum ratings for the eyTST-01 inputs

3 Operating conditions

See Table 3.

4 DUT Connectors

The connections for the DUT connectors C0 to C3 can be found in Appendix A.

5 DUT Power Supplies

The eight DUT Supplies (PS_0 through PS_7) source and sink 50 mA over a specified output voltage range of ±16.5 V. For low distortion, the supplies are linear regulated (for detailed Spec see Table 4). The linear regulators of the four supply channels PS_2, PS_3, PS_4 and PS_5 can be supplied via the additional input supplies called +USER and -USER. This option is available for extended currents up to 200 mA or extended voltage ranges up to ±18 V. Two considerations must be taken into account with DUT power supplies.

For low DUT voltages and high currents, the power dissipation in the sources is getting high. The additional board supplies called ±USER should be chosen to be roughly 5 V above the maximum voltage of PS_2, PS_3, PS_4 and PS_5. These board supplies also need to be used, if DUT voltages above ±16.5 V are anticipated. The maximum supply can be chosen to ±18 V. The extended supply input should be chosen to at least 5 V above the maximum DUT supply, but not higher than ±24 V. The short circuit current is typically 380 mA.

The currents sourced or sinked from the DUT supply can exceed the 50 mA based on Figure 4.

For good load regulation, the supplies utilize force and sense lines. The force line drives the supply current and should be wide enough on the DUT card to support the current drive capabilities. The sense line should be connected on the DUT card without any resistance close to the load. The source will remain stable without the sense line, but the load regulation performance will decrease. The DUT supply voltage is initially 0 V and connects to the DUT card without relay.

All eight DUT supply sources can be modulated with a signal for PSRR testing. This noise signal must be applied on the AC+ port.

Two ranges are available to measure the output current of the DUT supply via the measurement path. The initial range 0 can cover ±200 mA. An optional range up to 1 mA can be chosen.

The accuracy of the DUT supplies is specified in Table 4. The DUT supplies and the current measurement are calibrated. To avoid long-term drift, they should be re-calibrated annually.

Programmable temperature alert circuits are placed around the DUT supplies. They are initially set to 110 °C. All analog resources will shut down in case of an alert and an alarm window will pop up. For more information see the section on temperature alerts.

Parameter	Comment	Min	Typ	Max	Unit
+20V	to GND	19		21	V
-20V	to GND	-21		-19	V
+USER*	to GND	10		24	V
-USER*	to GND	-24		-10	V
+5V	to GND	4.5		5.5	V
Ambient Temperature		-40		85	°C

Table 3: Operating conditions for the eyTST-01
*Optional supplies. See section on DUT power supplies

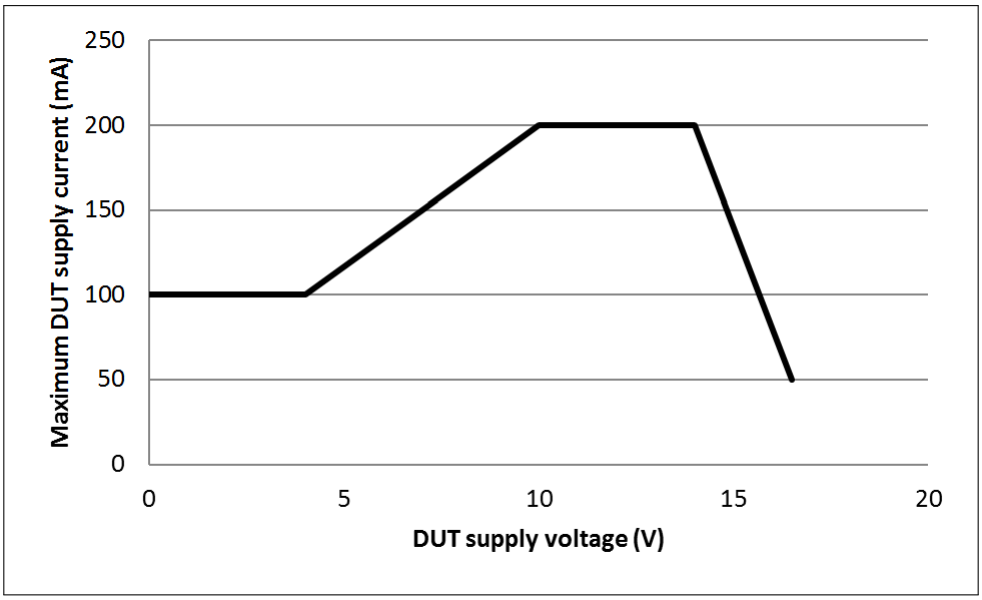

Figure 4: Maximum DUT supply output current versus DUT supply voltage

Parameter	Comment	Min	Typ	Max	Unit
Initial DUT supply voltage		-10		10	mV
DUT supply voltage accuracy	25°C	-1		1	mV
DUT supply voltage drift			50		ppm/°C
Load Regulation			10		μV/mA
Current measurement - Range 0				200	mA
Current measurement - Range 1				1	mA
Current measurement accuracy	25°C	-0.15		0.15	%FS
Current measurement accuracy		-0.25		0.25	%FS
Short circuit current			380		mA
Power supply rejection (DC)			72		dB

Table 4: Specifications of the DUT supplies

6 DUT Reference Sources

The DUT References (REF_0 through REF_3) source and sink 10 mA over a specified output voltage range of ±12 V. Based on Figure 5, higher load currents can be supported for reference voltages less than 12 V.

For good load regulation, the DUT references utilize force and sense lines. The force line drives the reference current. The sense line should be connected on the DUT card without any resistance close to the load. The source will remain stable without the sense line, but the load regulation performance will decrease. The DUT reference voltage is initially 0 V and connects to the DUT card without relay.

Two ranges are available to measure the output current of the DUT supply via the measurement path. The initial range 0 can cover ±20 mA while the optional range 1 supports ±200 μA.

The accuracy of the DUT references is specified in Table 5. The DUT references and the current measurement are calibrated. To avoid long-term drift, they

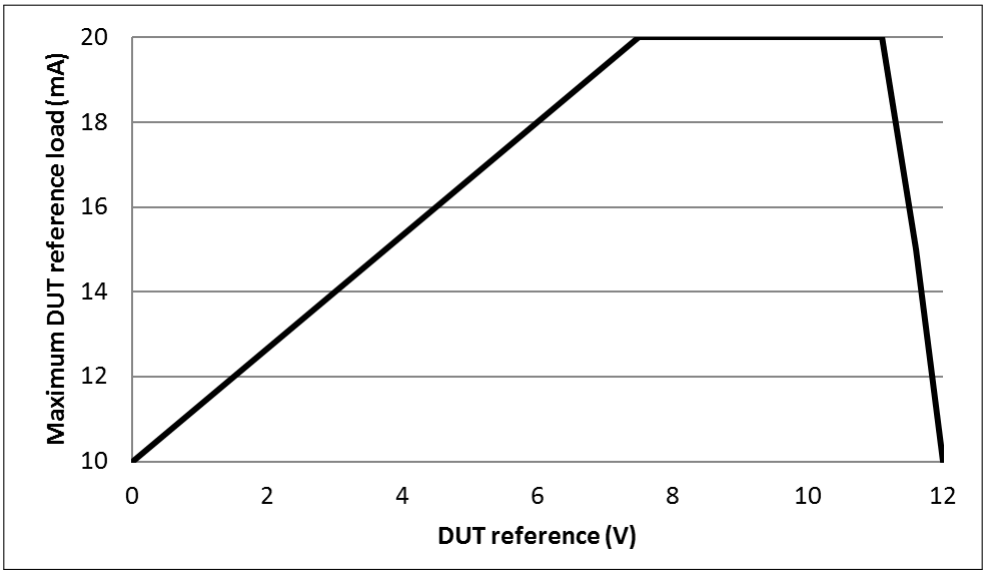

Figure 5: Maximum DUT reference load versus maximum DUT reference voltage

should be re-calibrated annually. The drift of the DUT reference has an amplitude independent portion and an amplitude dependent portion. The two components must be added to receive the total DUT reference drift.

7 Analog Signal Paths

The eyTST-01 has two signal paths - the AC and DC paths. Both paths provide external inputs via the BNC connectors called AC+ and AC- as well as DC+ and DC-. The paths provide the same signal conditioning circuitry, which is band-limited to 170 kHz for a maximum operating signal frequency of 100 kHz. The outputs, which connect to the contactor C0 (pins AC_P & AC_N and DC_P and DC_N) are buffered to provide a low impedance at a low noise level; the gain of the circuitry is 1.

The circuitry includes an optional single-ended (SE) to differential conversion so that single-ended or differential inputs can be accepted and single-ended or differential outputs can be provided. The common-mode level of the differential output voltage can be programmed separately for each path in a range of ±12 V. The performance of the signal paths is shown in Table 6. In order to achieve the given performance also single-ended or ground-referenced signals should be routed fully differential.

The differences of the two paths are explained in the following.

7.1 AC Signal Path

The AC path provides an optional band-pass filter of 6th order that has a center frequency at 2 kHz and a pass-band of 300 Hz. The filter can be used to provide a low distortion and low noise signal for circuits that operate at audio frequencies (see Table 7).

Parameter	Comment	Min	Typ	Max	Unit
DUT reference range		-12		12	V
Initial DUT reference voltage		-1		1	mV
DUT reference accuracy	25°C	-0.5		0.5	mV
DUT reference drift	amplitude dependent			10	ppm/°C
DUT reference drift	amplitude independent			6	μV/°C
Load				10	mA
Load Regulation			5		μV/mA
Current measurement - Range 0				200	μA
Current measurement - Range 1				10	mA
Current measurement accuracy	25°C	-0.15		0.15	% FS
Current measurement accuracy		-0.25		0.25	% FS
Noise			10		μV_{rms}
Noise	0.1-400Hz		3		μV_{rms}
Noise density	1kHz		5		nV/$\sqrt{\text{Hz}}$
Short circuit current			40		mA

Table 5: Specifications of the DUT references

Parameter	Comment	Min	Typ	Max	Unit
Input voltage range at AC+ and AC-		-12		12	V
Offset error		-1		1	mV
Offset error drift		-4		4	μV/°C
THD	amplitude ±10V, 10kHz, 2kΩ load		-110		dB
Noise	10kHz		10		nV/$\sqrt{\text{Hz}}$
Noise	1MHz		1.5		nV/$\sqrt{\text{Hz}}$
-3dB bandwidth			170		kHz
with SE to differential conversion:					
Offset error		-3		3	mV
Offset error drift		-8		8	μV/°C
Gain error [1]		-1.5		1.5	%
Gain error drift		-30		30	ppm/°C
THD	amplitude ±10V, 10kHz, 2kΩ load		90		dB
Common-Mode (CM) Voltage Range		-12		12	V
CM Voltage Accuracy		-1		1	mV

Table 6: Specifications of the AC and DC path

Parameter	Comment	Min	Typ	Max	Unit
Center frequency			2		kHz
Pass-band			300		Hz
Noise			TBD		μV_{pp}
THD			TBD		dB

Table 7: Specifications of the optional 2kHz band-pass filter

7.2 DC Signal Path

The DC path provides an optional high accuracy DC signal source, which can be used to drive the DC path instead of an external signal source that would connect to the BNC connectors DC+ and DC-.

The high accuracy signal source provides a programmable range of ±5 V or ±12.2 V. A fixed voltage can be programmed that follows the parameters specified in Table 8. A wait time of 0.1 s is required after switching from the ±5 V range to the ±12.2 V range or vice versa.

The DC Signal Path can also be programmed to provide a ramp with a specified start and end voltage at a certain steepness, which can be influenced by programming a step size of the signal source at a programmable update rate. High step sizes at a fast incrementation time will result in a steep ramp. On

the contrary, a low steepness can be achieved with a low step size and long incrementation times. The step size can be chosen as a multiple of 9.54 uV (±5 V range) or 24 uV (±12.2 V range). The incrementation time can be chosen in multiples of 1 us. Please note that switching process of the voltage source generates a glitch energy, which may influence the accuracy of the ramp for high slopes. In this situation it can be advantageous to increase the step size and increase the incrementation time (see Table 8).

Attached to the voltage source is an integrator that can integrate up or down with 1 μV/μs. The integrator voltage is added on top of the voltage source. It can be used for regulation loops, which are controlled by the FPGA. As an example, it can be used to regulate the voltage source to an anticipated transition voltage of an ADC or to the trigger voltage of a comparator. The threshold voltage can be directly measured with the measurement unit. The full-scale voltage of the integrator is ±120 mV (see Table 9).

The integrator can also run in a ramp mode, where it generates a ramp with an amplitude of ±8.3 mV. The ramp can, for example, be applied to a comparator including hysteresis, so that it repeats its operation continuously. The ramp is also connected to the BNC connector called X, so that it can be connected to the X input of an oscilloscope. The eyTST-01 also provides a fast 5 bit DAC (500 Ω output resistance), which can be controlled by the FPGA. The DAC connects to the BNC connector labeled as Y, which can be connected to the Y input of an oscilloscope. In this setup the transfer function of DUTs such as the comparator or ADC can be visualized on the oscilloscope (see Table 10 and 11).

8 Current Source

The current sources can source or sink 0 to ±100 mA with an output voltage range of ±12.2 V. The current can be set in steps of 3.2 μA (16 bit resolution). The accuracy of the current sources is specified in Table 12. The current sources are calibrated. To avoid long-term drift, they should be re-calibrated annually.

Figure 6 shows the safe operating area. This is given by the maximum internal power dissipation of the current source of 1.5 W. There is no internal thermal protection.

9 Measurement Unit

The eyTST-01 provides 8 differential DUT measurement channels through the contactor C1. They are labeled as MEAS_0 through MEAS_7. They can be chosen to connect to the measurement unit one at a time. The measurement unit is also utilized to measure the DUT supplies and DUT references and their output currents. This path is designed for low leakage currents less than 10 nA over the temperature from -40 °C to 85 °C.

Several options are provided inside the measurement path.

- Direct measurement with an external voltmeter connecting to the BNC connectors MEAS_P and MEAS_N
- Low impedance measurement with an external voltmeter connecting to MEAS_P and MEAS_N
- Internal high speed digitizer
- Internal high accuracy digitizer

The input of each path can be connected to ground, so that offsets can be calibrated at any time.

9.1 Direct Measurement Path

No active circuitry beside a multiplexer is connected between the 8 differential measurement channels and the output pins MEAS_P and MEAS_N. The leakage current is less than 10 nA over the full temperature range.

9.2 High Performance Measurement Path

A dedicated high performance measurement path is included for low noise AC measurements.

9.3 Buffered Measurement Path

In the case that there is risk of distortion through the wiring to the external voltmeter, the output impedance can be reduced to 50 Ω. The active conversion of the impedance is adding offset and offset drift (see Table 13).

The offset can be calibrated by applying a differential 0 V to the input of the low impedance measurement path first. This has to be done, before performing the required measurement.

9.4 Internal Digitizer

The two internal digitizers provide the selectable differential input voltage ranges that are listed in Table 14. The maximum voltage at the digitizer input should not exceed ±12.5 V.

The maximum signal frequency is limited to 15 kHz. The specified parameters for the two digitizers are listed below.

Parameter	Comment	Min	Typ	Max	Unit
Resolution			20		Bit
Voltage range (±4.9V):					
Bipolar zero error		-25		25	μV
Bipolar zero drift			2		μV/°C
Full scale error		-0.1		0.1	%
Full scale error drift			5		ppm/°C
Differential Linearity		-15		15	μV
Absolute Linearity		-15		15	μV
Noise	0.1 - 10Hz		15		μV_{pp}
Noise	1kHz		10		nV/$\sqrt{\text{Hz}}$
Minimum step size			9.5		μV
Incrementation time			1		μs
Voltage range (±12.2V):					
Bipolar zero error		-0.1		0.1	%
Bipolar zero drift			2		μV/°C
Full scale error		-50		50	μV
Full scale error drift			20		ppm/°C
Differential Linearity		-25		25	μV
Absolute Linearity		-40		40	μV
Noise	0.1 - 10Hz		25		μV_{pp}
Noise	1kHz		10		nV/$\sqrt{\text{Hz}}$
Minimum step size			24		μV
Incrementation time			1		μs

Table 8: Specifications of the signal source

Parameter	Comment	Min	Typ	Max	Unit
Integrator output range		-120		120	mV
Positive Slope			1		μV/μs
Negative Slope			-1		μV/μs

Table 9: Specifications of the signal source integrator

Parameter	Comment	Min	Typ	Max	Unit
Ramp output range		-8.3		8.3	mV
Positive Slope			10		μV/μs
Negative Slope			-10		μV/μs
Gain for X-Output			100		

Table 10: Specifications of the integrator in ramp mode

Parameter	Comment	Min	Typ	Max	Unit
Resolution		5			bits
Range		0		5	V
Output impedance			500		Ω
Coding	straight binary				

Table 11: Specifications of the 5bit DAC connecting to the Y output

9.4.1 High Speed Digitizer

See Table 15.

9.4.2 High Resolution Digitizer

See Table 16.

Parameter	Comment	Min	Typ	Max	Unit
Full scale range			±100		mA
DAC resolution			3.2		µA
Initial current (leakage)			±0.1	±10	µA
Absolute current accuracy			±4	±40	µA
Current offset error				±20	µA
Temperature drift	100mA			±50 5	ppm/K µA/K
Effective output resistance			20		MΩ
Output capacitance			50		pF
Output voltage range		-12.2		12.2	V
Absolute max. output voltage rating		-15		15	V

Table 12: Specifications of the current sources

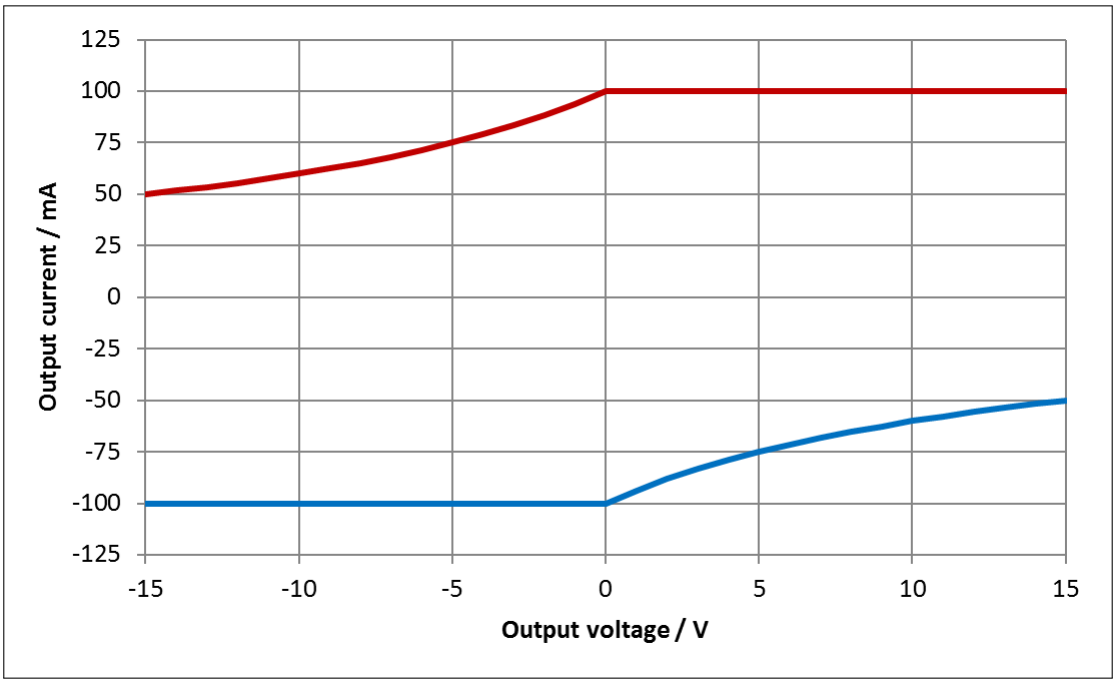

Figure 6: Safe current source operating area

Parameter	Comment	Min	Typ	Max	Unit
Output impedance			50		Ω
Offset error		-1.2		1.2	mV
Offset error drift			1		µV/°C

Table 13: Specifications of the low impedance measurement path

	Usable range		Full-scale range		
Range	Min	Max	Min	Max	Unit
0	-25	25	-40	40	V
1	-16	16	-20	20	V
2	-8	8	-10	10	V
3	-4	4	-5	5	V
4	-2	2	-2.5	2.5	V
5	-1	1	-1.25	1.25	V
6	-500	500	-625	625	mV
7	-250	250	-312.5	312.5	mV
8	-125	125	-156.25	156.25	mV
9	-62.5	62.5	-78.125	78.125	mV

Table 14: Input voltage ranges of internal digitizer

Parameter	Comment	Min	Typ	Max	Unit
Resolution		18			Bit
Range2					
Offset error		-100		100	μV
Offset error drift		-15		15	μV/°C
Gain error		-100		100	μV
Gain error drift			30		μV/°C
Noise			400		μV_{rms}
Signal frequency				15	kHz
Range9					
Offset error		-10		10	μV
Offset error drift		-1		1	μV/°C
Gain error		-10		10	μV
Gain error drift			7		μV/°C
Noise			10		μV_{rms}
Signal frequency				15	kHz

Table 15: Specifications of the high speed digitizer

Parameter	Comment	Min	Typ	Max	Unit
Resolution		24			Bit
Step response			300		ms
Range2					
Offset error		-50		50	μV
Offset error drift		-3		3	μV/°C
Gain error		-50		50	μV
Gain error drift			7		μV/°C
Noise			3		μV_{rms}
Signal frequency				15	kHz
Range9					
Offset error		-3		3	μV
Offset error drift		-0.2		0.2	μV/°C
Gain error		-3		3	μV
Gain error drift			8		μV/°C
Noise			0.1		μV_{rms}
Signal frequency				15	kHz

Table 16: Specifications of the high resolution digitizer

10 Temperature Alert

The eyTST-01 contains several circuits with high power dissipation such as the DUT supplies and the current sources. Temperature sensors are spread across the eyTST-01 to monitor a local increase in temperature. These sensors will trigger a temperature alert in case of local overheat and will shut the circuitry down after triggering a warning containing information regarding the location of the hot spot.

11 Electrical Overstress

As mentioned before electrical overstress can harm the board. This can occur in particular, if signal sources are applied to BNC connectors without applying the board supply. Therefore, the external connections are initially disconnected or are connected via some resistance to limit failure current. The external resources must be actively connected in the INIT portion of the test software.

12 Digital Resources

The DUT has 47 digital IO lines to the FPGA available. The used FPGA, Spartan-6 from Xilinx supports a huge list of I/O standards. The details can be found in the Xilinx SelectIO Resources documentation: www.xilinx.com/support/documentation/user_guides/ug381.pdf.

An SPI interface is available optionally to connect components on the DUT card such as the DUT or an EEPROM. Such an EEPROM might be used to support automatic detection of the DUT card from the software. If it is not used, the CS line could be used as standard digital IO.

The DUT can also be supplied with seven clock lines from the FPGA side. If they are not needed as a clock, the lines also can be used as digital IO lines. If they are used as clock lines, the Spartan-6 gives the possibility to use them as high performance, low skew clocking IO lines. The complete details can be found in the Xilinx Clocking Resources documentation: www.xilinx.com/support/documentation/user_guides/ug382.pdf.

The users can build their own DUT-PC interface by using the predefined OpalKelly endpoints inside the FPGA. A set of up to 16 okWireIn and up to 16 okWireOut endpoints are still available for that purpose. Additional 16 okTriggerIn and 16 okTriggerOut endpoints and 16 okPipeIn and 16 okPipeOut endpoints are available. An “in” endpoint is used to move data from PC to the FPGA (endpoint) and into the DUT. An “out” endpoint is used to move data from the DUT into the FPGA (endpoint) and out to the PC. The FPGA still has a host interface to initiate the USB 2.0 connection from the endpoints to the PC.

The okTriggerIn and okTriggerOut endpoints can be used to transmit a single shot synchronous transfer (e.g. events like conversion start). The okWireIn and okWireOut endpoints are used for transmitting small amount of data (e.g. configuration data). The okPipeIn and okPipeOut endpoints are used for the transfer of a larger amount of data (e.g. measurement data). The user needs to take care on the DUT-endpoint interface to ensure the data is delivered or collected as needed. The USB 2.0 interface between the endpoints and the PC software is already on the FPGA.

The endpoints need to be instantiated in the user’s VHDL code and need to be part of the FPGA bit stream. Also, DUT specific software needs to address these endpoints in order to access them. More information on using these endpoints can be found on the OpalKelly webpage: www.opalkelly.com/

13 Software

eyTST-01 comes with a software package that allows easy control of the hardware. The user can access each function on the board using a graphical user interface. Voltage, current and reference sources can be enabled and configured independently.

Once a device under test is configured concerning its stimuli and supplies, the setup can be saved for future use. This shortens setup times when several DUTs have to be processed in batch mode. When it comes to the debugging of a new design, it is advantageous to know, which stimulus was applied when. The software allows the user to log every stimulus change together with a timestamp, so that test fails can be reproduced easily.

Regarding automated tests, eyTST-01’s software package allows the user to control the test solution in a scripted way. Each test run can be fully customized using the software’s plugin interface. By using a user-generated script .dll (dynamic link library) it is possible to access each function on the test solution as if a user was clicking the GUI’s buttons. The live preview shows what is happening in real-time. All setup parameters of the test solution’s current state are visible at a glance. Each test case and/or DUT can have its own plugin, which can be archived for regression testing. Each DUT card can be identified by a unique number or identification string if the user

so wishes. This way the documentation of a test run becomes easier and less error-prone under the condition that each DUT sample has its own daughterboard.

The plugins can implement further GUIs, so that user specific analysis and data processing can be carried out (e.g. visually). On request, eesy-ic provides a software development kit with further data processing and visualization functions.

The user has direct access to the DUT through a certain amount of interfaces that are provided by the plugin interface. These interfaces are of the types trigger, pipe and wire as shown in Figure 7. Figure 7 describes the internal FPGA code structure.

The USB interface, eesy-ic interface and eyTST-01 control are blocks provided by eesy-ic, that control the board specific devices like voltage and current sources and measurement devices. The user specific block is anticipated for FPGA code that will be provided by the user. This block is the interface between the eesy-ic FPGA internal function control environment and the user's DUT. The block has direct access to the afore mentioned triggers, pipes and wires.

Triggers are 16 bit wide and designed for onetime events where, for example, a specific task has to be started. Wires are 16 bit wide and can be used to transmit configuration data or small amounts of data into the DUT. Pipes are also 16 bit wide and are used for the transmission of large amounts of data, such as sampled measurement data or binary coded waveforms, to a DAC. Following the pinout table, the user is able to connect these three types of interfaces to any of his DUT's interfaces, allowing direct DUT pin access.

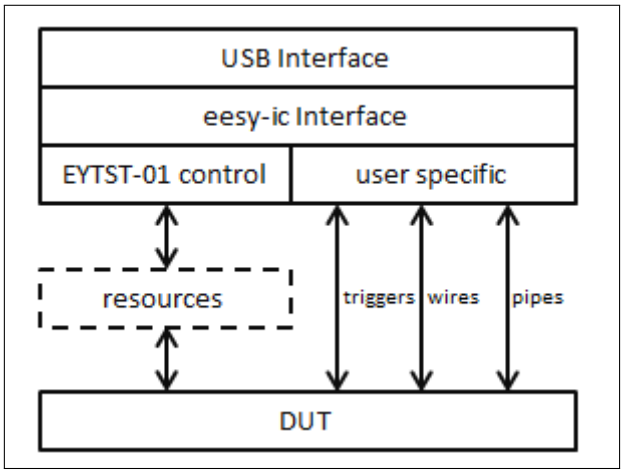

Figure 7: Firmware structure in VHDL/Verilog

Minimum requirements:

- Microsoft Windows compatible PC running Windows XP or 7 (32/64 bit)
- Intel Core i3 or compatible CPU
- 1 GB RAM
- 500 MB of free disk space
- 1280x800 pixel screen resolution
- USB 2.0 interface

Software requirements for plugin development:

- Microsoft Visual Studio (C# preferred)

14 Physical Outline

See Figure 8 and 9.

15 Document History

Rev 0.1; Date: 05/2013; Initial Preliminary Datasheet.
Rev 0.2; Date: 01/2014; Update Prelim. Datasheet.
Rev 0.3; Date: 01/2016; Adaption to revB, prelim. Datasheet.
Rev 0.4; Date: 09/2016; Mechanicals update, prelim. Datasheet.
Rev 0.5; Date: 07/2018; Digital interface correction, prelim. Datasheet.

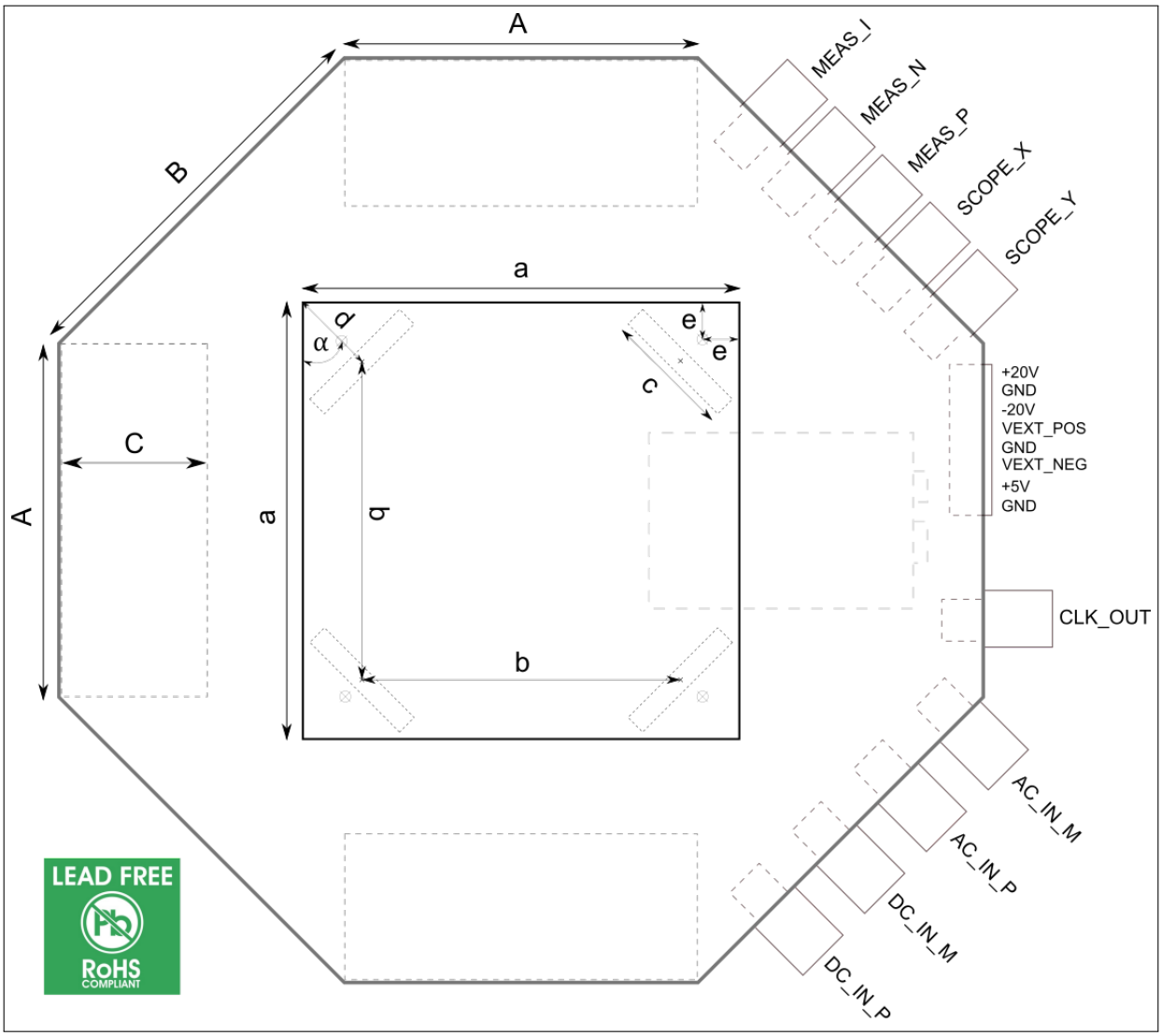

Figure 8: Physical outline of eyTST-01

EYTST-01		DUT card		Unit
A	100	a	124	mm
B	114.13	b	90	mm
C	41.5	c	37.27	mm
		d	24.04	mm
		α	45	°
⊗ Drill	3.2	e	9.5	mm

Figure 9: Physical dimensions of eyTST-01

A DUT connectors

Pin		Connector C0
No.	**Name**	**Pin description**
78	PS_3_F	DUT Power Supply 3. Force line.
76	PS_3_S	DUT Power Supply 3. Sense line.
72	PS_2_F	DUT Power Supply 2. Force line.
70	PS_2_S	DUT Power Supply 2. Sense line.
66	PS_1_F	DUT Power Supply 1. Force line.
64	PS_1_S	DUT Power Supply 1. Sense line.
60	PS_0_F	DUT Power Supply 0. Force line.
58	PS_0_S	DUT Power Supply 0. Sense line.
50	I_0	DUT Current Source 0
46	I_1	DUT Current Source 1
36	REF_0_F	Reference 0. Force line.
34	REF_0_S	Reference 0. Sense line.
30	REF_1_F	Reference 1. Force line.
28	REF_1_S	Reference 1. Sense line.
24	REF_2_F	Reference 2. Force line.
22	REF_2_S	Reference 2. Sense line.
18	REF_3_F	Reference 3. Force line.
16	REF_3_S	Reference 3. Sense line.
12	DC_P	DC Analog Signal Path. Non-inverting input.
10	DC_N	DC Analog Signal Path. Inverting input.
6	AC_P	AC Analog Signal Path. Non-inverting input.
4	AC_N	AC Analog Signal Path. Inverting input.
ELSE	GND	Ground connection.

Table 17: Pinout of connector C0

Pin		Connector C1
No.	**Name**	**Pin description**
3	MEAS_7_N	Measurement channel 7. Inverting input.
5	MEAS_7_P	Measurement channel 7. Non-inverting input.
9	MEAS_6_N	Measurement channel 6. Inverting input.
11	MEAS_6_P	Measurement channel 6. Non-inverting input.
15	MEAS_5_N	Measurement channel 5. Inverting input.
17	MEAS_5_P	Measurement channel 5. Non-inverting input.
21	MEAS_4_N	Measurement channel 4. Inverting input.
23	MEAS_4_P	Measurement channel 4. Non-inverting input.
27	MEAS_3_N	Measurement channel 3. Inverting input.
29	MEAS_3_P	Measurement channel 3. Non-inverting input.
33	MEAS_2_N	Measurement channel 2. Inverting input.
35	MEAS_2_P	Measurement channel 2. Non-inverting input.
39	MEAS_1_N	Measurement channel 1. Inverting input.
41	MEAS_1_P	Measurement channel 1. Non-inverting input.
45	MEAS_0_N	Measurement channel 0. Inverting input.
47	MEAS_0_P	Measurement channel 0. Non-inverting input.
51	HPERF_P	High performance channel. Non-inverting input.
53	HPERF_N	High performance channel. Inverting input.
57	PS_7_F	DUT Power Supply 7. Force line.
59	PS_7_S	DUT Power Supply 7. Sense line.
63	PS_6_F	DUT Power Supply 6. Force line.
65	PS_6_S	DUT Power Supply 6. Sense line.
69	PS_5_F	DUT Power Supply 5. Force line.
71	PS_5_S	DUT Power Supply 5. Sense line.
75	PS_4_F	DUT Power Supply 4. Force line.
77	PS_4_S	DUT Power Supply 4. Sense line.
ELSE	GND	Ground connection.

Table 18: Pinout of connector C1

Pin		FPGA port	Connector C2
No.	**Name**		**Pin description**
2	3.3V		3.3V FPGA communication supply
3	CLK_4	B10	Digital Clock line 4. Can also be used as digital IO.
5	D25	W22	Digital IO pin 25.
7	D26	U19	Digital IO pin 26.
9	D27	V20	Digital IO pin 27.
11	D28	C5	Digital IO pin 28.
13	D29	A5	Digital IO pin 29.
15	D30	D14	Digital IO pin 30.
17	D31	C14	Digital IO pin 31.
20	3.3V		3.3V FPGA communication supply
21	CLK_5	A10	Digital Clock line 5. Can also be used as digital IO.
23	D32	E16	Digital IO pin 32.
25	D33	D17	Digital IO pin 33.
27	D34	D7	Digital IO pin 34.
29	D35	D8	Digital IO pin 35.
31	D36	L17	Digital IO pin 36.
33	D37	K18	Digital IO pin 37.
35	D38	D6	Digital IO pin 38.
38	3.3V		3.3V FPGA communication supply
39	CLK_6	C11	Digital Clock line 6. Can also be used as digital IO.
41	D39	C6	Digital IO pin 39.
43	D40	A3	Digital IO pin 40.
45	D41	A4	Digital IO pin 41.
47	D42	B8	Digital IO pin 42.
49	D43	A8	Digital IO pin 43.
51	D44	C13	Digital IO Pin 44.
53	D45	A13	Digital IO pin 45.
56	3.3V		3.3V FPGA communication supply
57	CLK_7	A11	Digital Clock line 7. Can also be used as digital IO.
59	D46	C15	Digital IO pin 46.
61	D47	A15	Digital IO Pin 47.
63	D48	C17	Digital IO pin 48.
65	NC		Do not connect.
70	3.3V		3.3V FPGA communication supply
73	REL_0		DUT Relay Driver 0. Current sink.
74	5V		5V supply for relay coil.
75	REL_1		DUT Relay Driver 1. Current sink.
76	5V		5V supply for relay coil.
77	REL_2		DUT Relay Driver 2. Current sink.
78	5V		5V supply for relay coil.
79	REL_3		DUT Relay Driver 3. Current sink.
80	5V		5V supply for relay coil.
ELSE	GND		Ground connection.

Table 19: Pinout of connector C2

Pin		FPGA port	Connector C3
No.	**Name**		**Pin description**
2	3.3V		3.3V FPGA communication supply
3	SPI_CLK	D11	Serial Port Interface (SPI). Clock line.
5	SPI_CS	T20	DUT Board SPI. Frame Synchronization line.
7	SPI_SDI	T19	DUT Board SPI. Serial Data In line.
9	D1/SDO	P17	Digital IO pin 1. Can be used as Serial Data Out Line.
11	D2/CS2	N16	Digital IO pin 2. Can be used as additional CS line.
13	D3	M17	Digital IO pin 3.
15	D4	M18	Digital IO pin 4.
17	D5	P18	Digital IO pin 5.
20	3.3V		3.3V FPGA communication supply
21	CLK_1	C12	Digital Clock line 1. Can also be used as digital IO.
23	D6	R19	Digital IO pin 6.
25	D7	D9	Digital IO pin 7.
27	D8	C8	Digital IO pin 8.
29	D9	D10	Digital IO pin 9.
31	D10	C10	Digital IO pin 10.
33	D11	D15	Digital IO pin 11.
35	D12	C16	Digital IO pin 12.
38	3.3V		3.3V FPGA communication supply
39	CLK_2	B12	Digital Clock line 2. Can also be used as digital IO.
41	D13	B6	Digital IO pin 13.
43	D14	A6	Digital IO pin 14.
45	D15	C7	Digital IO pin 15.
47	D16	A7	Digital IO pin 16.
49	D17	C9	Digital IO pin 17.
51	D18	A9	Digital IO Pin 18.
53	D19	B14	Digital IO pin 19.
56	3.3V		3.3V FPGA communication supply
57	CLK_3	A12	Digital Clock line 3. Can also be used as digital IO.
59	D20	A14	Digital IO pin 20.
61	D21	B16	Digital IO Pin 21.
63	D22	A16	Digital IO pin 22.
65	D23	B18	Digital IO pin 23.
67	D24	W20	Digital IO pin 24.
70	3.3V		3.3V FPGA communication supply
73	REL_4		DUT Relay Driver 4. Current sink.
74	5V		5V supply for relay coil.
75	REL_5		DUT Relay Driver 5. Current sink.
76	5V		5V supply for relay coil.
77	REL_6		DUT Relay Driver 6. Current sink.
78	5V		5V supply for relay coil.
79	REL_7		DUT Relay Driver 7. Current sink.
80	5V		5V supply for relay coil.
ELSE	GND		Ground connection.

Table 20: Pinout of connector C3

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